PAPER ID-310875

Subject Code: KEC054

Roll No: | | | | | | | | | | | | | |

BTECH

(SEM V) THEORY EXAMINATION 2023-24

ADVANCE DIGITAL DESIGN USING VERILOG

TIME: 3 HRS **M.MARKS: 100**

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. **2 x 10 = 20**

Qno.	Question	Marks	CO
a.	What is don't care handling?	2	1
b.	What is meant by combinational logic?	2	1
c.	What do you mean by comparator?	2	2
d.	What is elimination of hazards?	2	2
e.	Give an example of a synchronous circuit	2	3
f.	What is Asynchronous Sequential Circuit Design?	2	3
g.	Define fault sensitization	2	4
h.	What is the use of initial in Verilog code?	2	4
i.	What are 4 basic elements of FPGA?	2	5
j.	What does PLA stand for?	2	5

SECTION B

2. Attempt any *three* of the following: **10 x 3 = 30**

a.	Describe the XOR Pattern handling in digital design.	10	1
b.	Describe the techniques and methods used in structural specifications logic circuits with Verilog	10	2
c.	Explain the working of ASM charts	10	3
d.	Explain the working of BDD in digital design.	10	4
e.	Draw and explain the architecture of ASIC	10	5

SECTION C

3. Attempt any *one* part of the following: **10 x 1 = 10**

a.	Explain mixed logic in digital design	10	1
b.	Explain Logic Representation and Minimization with cost in digital design	10	1

4. Attempt any *one* part of the following: **10 x 1 = 10**

a.	Discuss Behavioral and Structural specification of logic circuits	10	2
b.	How Boolean function are implementation using Verilog?	10	2

5. Attempt any *one* part of the following: **10 x 1 = 10**

a.	Explain Mapping Algorithm	10	3
b.	Discuss Multi-level minimization and optimization.	10	3

6. Attempt any *one* part of the following: **10 x 1 = 10**

a.	Explain Fault Detection and Analysis in combinational and sequential systems	10	4
b.	What is Factoring? Discuss Binary decision diagram.	10	4

7. Attempt any *one* part of the following: **10 x 1 = 10**

a.	Explain the design of Combinational circuit using CPLD.	10	5
b.	How a sequential circuit can be designed using FPGA?	10	5