PAPER ID-310872

Subject Code: KEC051

Roll No: | | | | | | | | | | | | | |

BTECH

(SEM V) THEORY EXAMINATION 2023-24

COMPUTER ARCHITECTURE AND ORGANIZATION

TIME: 3 HRS **M.MARKS: 100**

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. **2 x 10 = 20**

Q no.	Question	Marks	CO
a.	Compare combinational and sequential logic circuits.	2	1
b.	Explain the use of program counter.	2	3
c.	Compare PLA and PAL.	2	2
d.	Describe Moore's law.	2	1
e.	Write the differences between EPROM, EEPROM and flash memory.	2	5
f.	Represent (– 320) decimal number in both binary sign magnitude and two's complement using 16 bits.	2	1
g.	Describe floating point number representation with an example.	2	4
h.	Compare combinational and sequential logic circuits.	2	1
i.	Differentiate between cache memory and RAM.	2	5
j.	Compare SRAM with DRAM.	2	4

SECTION B

2. Attempt any *three* of the following: **10 x 3 = 30**

a.	Explain following in detail: i. Encoder and Decoder ii. Virtual address and Physical address	10	1
b.	Draw and explain CPU instruction cycle with interrupts.	10	2
c.	Show the multiplication process using Booth algorithm, when the following binary numbers, (+12) x (-16) are multiplied.	10	3
d.	Discuss different pipeline hazards in detail.	10	4
e.	Discuss different type of secondary memories.	10	5

SECTION C

3. Attempt any *one* part of the following: **10 x 1 = 10**

a.	What is addressing mode? Explain any five with suitable example.	10	1
b.	Define the two approaches used to deal with multiple interrupts. Also write their disadvantages.	10	1

4. Attempt any *one* part of the following: **10 x 1 = 10**

a.	Find the following difference using 8-bit two's complement arithmetic. Show steps and also write decimal value of the difference. Why two's complement arithmetic is better? (28 – 45)	10	2
b.	Draw the diagram of expanded structure of IAS computer and explain its blocks.	10	2

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5. Attempt any *one* part of the following: 10 x 1 = 10

a.	Briefly define the seven RAID levels. How is redundancy achieved in these RAID systems?	10	3
b.	Draw the structure of DRAM binary cell and explain how binary digits are written and read from it?	10	3

6. Attempt any *one* part of the following: 10 x 1 = 10

a.	Explain how the performance of a processor can be improved by increasing microprocessor speed, balancing performance of various components and improving chip design?	10	4
b.	Why multiple buses are used in any computer system? Name common Multiple-Bus Hierarchies and explain one of them with proper diagram.	10	4

7. Attempt any *one* part of the following: 10 x 1 = 10

a.	Name all the elements that are essential for cache design. Discuss replacement algorithms in detail.	10	5
b.	What is mapping function? Explain direct mapping method with the help of an example. Differentiate between Direct and Associative mapping.	10	5