PAPER ID-311728

Roll No:

BTECH
(SEM III) THEORY EXAMINATION 2023-24
ELECTRONIC DEVICES

TIME: 3HRS   **M.MARKS: 70**

Note: Attempt all Sections. If require any missing data, then choose suitably.

SECTION A

1.   **Attempt *all* questions in brief.**

Q no.	Question	Marks
a.	Discuss thermal Equilibrium Condition.	2
b.	Illustrate the energy band diagram for PN junction in reverse mode.	2
c.	A transistor has an α of 0.98. Determine the value of β.	2
d.	Illustrate Electroluminescence.	2
e.	State the de Broglie principle of duality.	2
f.	Write properties of MOS capacitor.	2
g.	Differentiate between drift and diffusion current.	2

SECTION B

2.   **Attempt any *three* of the following:**

a.	Explain photoelectric effect. justify how this effect verifies the particle nature of light.	7
b.	Illustrate Intrinsic and Extrinsic Semiconductor in detail.	7
c.	Explain the small signal model of PN-Junction Diode	7
d.	Describe stability factor and explain how it affect the transistor biasing.	7
e.	Explain the C-V Characteristic of MOS Transistor.	7

SECTION C

3.   **Attempt any *one* part of the following:**

a.	Discuss Application of Schrödinger wave equation for infinite Potential well and discuss the effect of various in relation to the energy of the particle.	7
b.	Illustrate the concept of allowed and forbidden energy bands in a single crystal both qualitatively and more rigorously from the results of using the Kronig–Penney model.	7

4.   **Attempt any *one* part of the following:**

a.	Define the term Doping. Explain the effect of Impurity on energy band gap Diagram in detail.	7
b.	Using the concept of drift and diffusion of carriers, derive the continuity equation.	7

5.   **Attempt any *one* part of the following:**

a.	Describe the importance of Einstein relation and prove the relation.	7
b.	Derive the relation of voltage and current for PN junction diode.	7

6.   **Attempt any *one* part of the following:**

a.	Explain Ebers-Moll model for PNP transistor.	7
b.	Name the different biasing schemes used transistor biasing. Explain voltage divider biasing in detail.	7

7.   **Attempt any *one* part of the following:**

a.	Explain various biasing schemes for JFET.	7
b.	Explain Enhancement P channel MOSFET in detail. Draw and elaborate the drain Characteristic	7