**Printed Pages: 2** **Sub Code:KOE049**

**Paper Id:** 238145 **Roll No.** | | | | | | | | | | |

# B. TECH.
# (SEM IV) THEORY EXAMINATION 2022-23
# DIGITAL ELECTRONICS

***Time: 3 Hours*** ***Total Marks: 100***

**NOTE: 1.** Attempt all Sections. If require any missing data, then choose suitably.

## SECTION A

**1. Attempt *all* questions in brief. 2 x 10 = 20**

(a) Interpret the binary number $(1011)_2$ into (i) Gray code (ii) Excess-3 Code.
(b) Evaluate $(1011)_2$ - $(1101)_2$ using 1's and 2's complement method.
(c) Differentiate between the serial and parallel adder.
(d) How many 4 X 1 multiplexers are required to implement 64 X 1 multiplexer.
(e) What is the difference between characteristic and excitation table.
(f) Differentiate between combinational and sequential circuits.
(g) How many address lines are needed to represent 8K meaning.
(h) Define term propagation delay.
(i) Define race around condition in JK flip flop.
(j) Give the difference between PAL and PLA.

## SECTION B

**2. Attempt any *three* of the following: 10x3=30**

(a) Implement the Boolean function F(x,y,z)=(1,2,3,4,6,7) using NAND gates.
(b) Construct a full adder and implement the full adder with the help of half adders. Also implement the full adder with NAND gates only.
(c) Discuss excitation table for SR, JK, T and D flip flop.
(d) Design 8Kx8 RAM memory system, using 1Kx8 memory ICs.
(e) Discuss Mealy and Moore finite state machine with an example.

## SECTION C

**3. Attempt any *one* part of the following: 10x1=10**

(a) Simplify Y=∑m (3,6,7,8,10,12,14) + d (0,1,6,15) using K-map method and implement the simplified circuit using logic gates.
(b) Minimize the following Boolean function using tabulation method:
F (a,b,c,d,e) = ∑ m (0,4,12,16,19,24,27,28,29,31)

**4. Attempt any *one* part of the following: 10x1=10**

(a) Design a BCD adder using 4-bit parallel adder.
(b) Draw and Explain 2-bit magnitude comparator. Also represent output with the help of logic diagram.

**5. Attempt any *one* part of the following: 10x1=10**

(a) Design and implement MOD-10 synchronous counter.

(b) For the clocked JK Flip-Flop write the state table, state equation with state diagram.

**6. Attempt any *one* part of the following: 10x1=10**

(a) Why ECL is better? Implement NAND gate with DTL and TTL.

(b) Define noise margin, Fan-in, Fan-out as characteristics of logic families. Implement NAND gate with CMOS.

**7. Attempt any *one* part of the following: 10x1=10**

(a) Explain State Reduction and assignment with suitable example.

(b) Design a sequential circuit with two flip flops, A & B and one input X. When X=0 state of the circuit remains the same, when X =1 circuit passes through the state transition from 00 to 01 to 11 to 10 back to 00 and repeat.